CLAIMS:

1. A system for keeping time in a clock domain, comprising:

a free-running clock domain having:

a first latch coupled to the output of the free-running clock;

an inverter coupled to the output of the first latch; and

a core mesh-clock domain having:

at least one or more secondary latches coupled to the output of the first latch;

an edge detector coupled to the output of the secondary latches;

an incrementer coupled to the output of the edge detector; and

a memory coupled to the output of the incrementer.

2. The system of Claim 1, wherein the secondary latches comprise at least two latches coupled in series.

3. The system of Claim 1, wherein an output of the memory is coupled to the input of the incrementer.

4. The system of Claim 1, wherein the free-running clock is running at an frequency different than the core mesh-clock.

5. The system of Claim 1, wherein the memory is employable as a storage device for measuring the passage of time.

6. The system of Claim 1, wherein the first latch outputs a digital value.

7. The system of Claim 1, wherein there is a single signal line between the first latch and the one or more secondary latches that crosses between the free-running clock domain and the core mesh-clock domain.

8. The system of Claim 1, wherein the memory is incrementing at a frequency slower than the free-running clock is incrementing.

9. A method of generating a constant time incremental change, comprising:

generating a clock pulse;

generating a voltage level from the clock pulse;

delaying the voltage level;

detecting an edge on the voltage level; and

incrementing a value based upon an edge detection.

10. The method of Claim 9, wherein the increment value represents a second clock frequency.

11. The method of Claim 9, wherein the voltage level is inverted and input into a latch.

12. The method of Claim 9, wherein the value is stored in a memory.

13. The method of Claim 12, wherein the output of the memory is used by the incrementer to increment to the next value.

14. The method of Claim 9, wherein the step of delaying the voltage signal employs a plurality of latches in series.

15. The method of Claim 9, wherein the incrementer employs an n-bit adder.

16. The method of Claim 9, wherein the clock frequency and the core mesh-clock frequency are not the same frequency.

17. The method of Claim 9, wherein an enable signal is conveyed to the clock.